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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
MATTHEW, AARON D	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,218	THOMPSON ET AL.	
	Examiner	Art Unit	
	Aaron D Matthew	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-14 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-14 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 6, 7, 15, and 16 have been cancelled.

2. Claims 1-5, 8-14, and 17-21 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 8-14, and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair, (US 6,318,965 B1), and further in view of Sekiguchi, (US 6,398,505 B1), White, (US 2002/0010881), and Beeghly, (US 4,336,463).

Regarding claim 1, Nair teaches a computer system comprising:

- A host processor, (see Fig. 2, element 62);
- A plurality of fan controllers coupled to said host processor, (see Fig. 2, elements 56 and 57); and
- A fan coupled to each fan controller, (see Fig. 2, elements 76 and 60);

Nair fails to teach that said fan controllers are inter-connected by a fault signal which is used to transmit fault information between the fan controllers without host processor involvement. However, Nair does teach a need for a fan which can interface directly with one or more fans to optimize fan performance, (see col. 1, lines 55-60).

Sekiguchi teaches a cooling apparatus for use in a computer system, comprising a plurality of fan controllers, wherein the fan controllers are inter-connected by a fault signal that is used to transmit fault information between the fan controllers, (see col. 4, lines 15-20, col. 6, lines 59-67, and col. 8, lines 40-49), without host processor involvement, (note that "monitoring portion 5", of Fig. 2, is independent of a host processor).

Sekiguchi and Nair are analogous art because they are from the same field of endeavor, viz., the operation of fan controllers in a computer system.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the intercommunicating fan controllers of Sekiguchi with the computer cooling system of Nair, in order to achieve a cooling system in a system comprising a host processor, in which a plurality of fan controllers are capable of relaying fault information without host processor involvement.

One of ordinary skill in the art would have been motivated to combine the teachings because the cooling system of Sekiguchi offers distinct advantages over the teachings of Nair. Note col. 13, lines 35-39, of Sekiguchi, which disclose that the independence of each of the plurality of the fan controllers taught therein reduces maintenance costs in the cooling system. Also, by enabling fault signal communication between the independent fan controllers, the overall cooling power of the system is not necessarily reduced as a result of failure of a single fan unit, (see col. 4, lines 38-47). Therefore, one of ordinary skill in the art would have been clearly motivated to combine the intercommunicating fan controllers of Sekiguchi with the computer cooling system of Nair in order to prevent loss of overall cooling power in the event of a fan failure, and to reduce maintenance costs resulting from said failure.

Nair, in view of Sekiguchi, fails to disclose that each fan controller comprises a register that includes a bit that can be set by said host processor to cause said fan controller to not assert said fault signal upon detection of a fault.

White teaches a computer system comprising a cooling fan, in which a fan unit comprises a register, (see par. 0077), which the host processor can access to control whether a fan unit asserts a fault signal, (see par. 0079, note that the register

disclosed in White includes a "RQST FAIL" bit, which is used to enable the indication of a failure of the cooling element).

Beeghly teaches a device comprising a cooling system, (see col. 1, lines 44-47), wherein a disable signal is output in order to prevent a fault signal from being asserted.

Nair, Sekiguchi, White and Beeghly are analogous art because they are all from the same problem solving area, viz., computing devices comprising cooling system control and means of asserting a fault signal based on a temperature sensor reading.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fan unit register field of White, with the fan controller system of Nair, in view of Sekiguchi, in order to improve the host processor's ability to control the functions of the fan controllers in the event of a cooling system failure.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the disable signal, taught in Beeghly, with the register of Nair, in view of Sekiguchi and White, in order to provide a bit, like the

"RQST FAIL" bit of White, within said register that would disable the assertion of a fault signal from a fan controller.

One of ordinary skill in the art would have been motivated to combine the teachings of White with the system disclosed in Nair, in view of Sekiguchi, because the register of White provides an easily transferable means of utilizing the non-volatile memory, disclosed on col. 4, lines 1-6 of Nair, to provide fault source information control to the host processor. One of ordinary skill in the art would have been motivated to combine the register of White with the non-volatile memory of Nair in order to enable host processor access to control the generation of fault source information. Further motivation is found in the teachings of Beeghly. Both White and Beeghly disclose that there are conditions in fault recognition systems wherein it is undesirable to assert a fault signal, (see White, par. 0079, and Beeghly, col. 2, lines 42-47). White shows that a fan unit can be disabled from asserting a fault signal that would turn on a visual fault indicator, but Beeghly shows that a fault signal should be disabled from being asserted during certain system conditions wherein such a fault signal could have been asserted erroneously, such as during system start-up. Therefore, one of ordinary skill in the art would have been motivated to combine fault signal disabling, as taught in Beeghly, with the register of Nair, in view of Sekiguchi and White, in order to prevent asserting a possibly erroneous fault signal during system conditions such as system start-up.

Regarding claim 5, see White, par. 0077; also note par. 0082, particularly lines 4-6.

Regarding claim 10, Nair discloses a fan controller comprising:

- An interface to controlling logic, (see col. 2, lines 30-35);
- An interface to a fan which permits said fan controller to control the speed of said fan, (see col. 2, lines 40-50); and
- A programmable register accessible by a host processor via said controlling logic, (see col. 3, lines 34-38);

Nair fails to disclose that said fan controller also comprises an input/output fault signal adapted to be coupled to another fan controller through which fault information can be shared between fan controllers without host processor involvement. However, Nair does teach a need for a fan which can interface directly with one or more fans to optimize fan performance, (see col. 1, lines 55-60).

Sekiguchi teaches a cooling apparatus for use in a computer system, comprising a plurality of fan controllers, wherein the fan controllers are inter-connected by an input/output fault signal that is used to transmit fault information between the fan controllers, (see col. 4, lines 15-20, col. 6, lines 59-67, and col. 8, lines 40-49), without host processor involvement, (note that "monitoring portion 5", of Fig. 2, is independent of a host processor).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the intercommunicating fan controllers of Sekiguchi with the computer cooling system of Nair, in order to achieve a cooling system in a system comprising a host processor, in which a plurality of fan controllers are capable of relaying fault information without host processor involvement.

One of ordinary skill in the art would have been motivated to combine the teachings because the cooling system of Sekiguchi offers distinct advantages over the teachings of Nair. Note col. 13, lines 35-39, of Sekiguchi, which disclose that the independence of each of the plurality of the fan controllers taught therein reduces maintenance costs in the cooling system. Also, by enabling fault signal communication between the independent fan controllers, the overall cooling power of the system is not necessarily reduced as a result of failure of a single fan unit, (see col. 4, lines 38-47). Therefore, one of ordinary skill in the art would have been clearly motivated to combine the intercommunicating fan controllers of Sekiguchi with the computer cooling system of Nair in order to prevent loss of overall cooling power in the event of a fan failure, and to reduce maintenance costs resulting from said failure.

Nair, in view of Sekiguchi, fails to disclose that said register includes a bit that can be set by said host processor to cause said fan controller to not assert said input/output fault signal upon detection of a fault.

White teaches a computer system comprising a cooling fan, in which a fan unit comprises a register, (see par. 0077), which the host processor can access to control whether a fan unit asserts a fault signal, (see par. 0079, note that the register disclosed in White includes a "RQST FAIL" bit, which is used to enable the indication of a failure of the cooling element).

Beeghly teaches a device comprising a cooling system, (see col. 1, lines 44-47), wherein a disable signal is output in order to prevent a fault signal from being asserted.

Nair, Sekiguchi, White and Beeghly are analogous art because they are all from the same problem solving area, viz., computing devices comprising cooling system control and means of asserting a fault signal based on a temperature sensor reading.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fan unit register field of White, with the fan controller of Nair, in view of Sekiguchi, in order to improve the host processor's

ability to control the functions of the fan controller in the event of a cooling system failure.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the disable signal, taught in Beeghly, with the register of Nair, in view of Sekiguchi and White, in order to provide a bit, like the "RQST FAIL" bit of White, within said register that would disable the assertion of a fault signal from a fan controller.

One of ordinary skill in the art would have been motivated to combine the teachings of White with the controller disclosed in Nair, in view of Sekiguchi, because the register of White provides an easily transferable means of utilizing the non-volatile memory, disclosed on col. 4, lines 1-6 of Nair, to provide fault source information control to the host processor. One of ordinary skill in the art would have been motivated to combine the register of White with the non-volatile memory of Nair in order to enable host processor access to control the generation of fault source information. Further motivation is found in the teachings of Beeghly. Both White and Beeghly disclose that there are conditions in fault recognition systems wherein it is undesirable to assert a fault signal, (see White, par. 0079, and Beeghly, col. 2, lines 42-47). White shows that a fan unit can be disabled from asserting a fault signal that would turn on a visual fault indicator, but Beeghly shows that a fault signal should be disabled from being asserted during certain system conditions

wherein such a fault signal could have been asserted erroneously, such as during system start-up. Therefore, one of ordinary skill in the art would have been motivated to combine fault signal disabling, as taught in Beeghly, with the register of Nair, in view of Sekiguchi and White, in order to prevent asserting a possibly erroneous fault signal during system conditions such as system start-up.

Regarding claim 14, see White, par. 0077; also note par. 0082, particularly lines 4-6.

Regarding claims 2, 3, 11 and 12, note that Sekiguchi teaches that when a fault signal, indicating a fan fault condition, is sent from one fan controller, another fan controller receives the fault signal and responds by increasing the speed of its fan, (see col. 2, lines 27-35).

Regarding claims 4 and 13, see Sekiguchi, Fig. 2, element 5, wherein the monitoring portion functions as a bridge.

Regarding claims 8 and 17, see Sekiguchi, col. 6, lines 59-67.

Regarding claims 9 and 18, see par. 0082 of White, wherein the register comprises a fan speed value.

Claims 19-21 are rejected because they recite limitations similar to claims 1-3, except in the context of a method of controlling fans in a computer system. Please see the discussion regarding claims 1-3.

Response to Arguments

4. Applicant's arguments, see page 7, section I., filed 12/27/2004, with respect to SPECIFICATION OBJECTIONS have been fully considered and are persuasive. The objection of specification has been withdrawn.

5. Applicant's arguments filed 12/27/2004, regarding THE ART REJECTIONS, on page 8, have been fully considered but they are not persuasive.

Regarding independent claims 1, 10 and 19, applicant argues that, "Beeghly clearly represents non-analogous art and, as such, cannot be used to reject," the claims. The applicant states that the "subject matter of Beeghly (internal combustion engines) has nothing to do with Applicants' field of endeavor (fan control techniques and associated apparatus for computers)." The examiner respectfully disagrees.

As was shown above in the discussion regarding claims 1 and 10, Beeghly, Nair, Sekiguchi, and White all represent analogous art because they are from the same

field of endeavor, viz., computing devices comprising cooling system control and means of asserting a fault signal based on a temperature sensor reading.

Applicant states that Beeghly's field of endeavor is internal combustion engines. However, though the subject matter does pertain to internal combustion engines, it would be more appropriate to identify Beeghly's field of endeavor as annunciators, which are electrical devices for giving an audible and visible signal. It is in the capacity that the examiner has determined Beeghly as being analogous art.

Nair, Sekiguchi, and White all utilize sensors in a computer system to monitor environmental temperature conditions, with the intent of triggering an alarm in the event of abnormal conditions. White, in particular, teaches a visual indicator to indicate a failure of a cooling element (associated directly with a high temperature reading, see par. 0079). Since Beeghly is concerned with the generation of an audible and visible indicator of high temperature conditions in a computerized system, (see Beeghly, col. 1, lines 44-50, and col. 2, lines 42-46), one of ordinary skill in the art would look to Beeghly for solutions to controlling fault signals generated by sensors in elevated environmental temperature conditions.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (571) 272-3662. The examiner can normally be reached on Mon-Fri, from 8:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aaron D Matthew
Examiner
Art Unit 2114

ADM

SCOTT BADERMAN
PRIMARY EXAMINER